Nanoscale Memory Elements Based on Solid-State Electrolytes

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***Abstract*—We report on the fabrication and characterization of nanoscale memory elements based on solid electrolytes. When combined with silver, chalcogenide glasses such as Se-rich Ge–Se are good solid electrolytes, exhibiting high Ag ion mobility and availability. By placing an anode that has oxidizable Ag and an inert cathode (e.g., Ni) in contact with a thin layer of such a material, a device is formed that has an intrinsically high resistance, but which can be switched to a low-resistance state at small voltage via reduction of the silver ions. An opposite bias will return the device to a high-resistance state, and this reversible switching effect is the basis of programmable metallization cell technology. In this paper, electron beam lithography was used to make sub-100-nm openings in polymethylmethacrylate layers used as the dielectric between the device electrodes. The solid electrolyte film was formed in these via-holes so that their small diameter defined the active switching area between the electrodes. The Ag–Ge–Se electrolyte was created by the photodiffusion, with or without thermal assistance, of an Ag layer into the Ge–Se base glass. Combined thermal and photodiffusion leads to a nanophase separated material with a dispersed Ag ion-rich material with an average crystallite size of 7.5 nm in a glassy insulating Ge-rich continuous phase. The nanoscale devices write at an applied bias as low as 0.2 V, erase by −0.5 V, and fall from over 10^7 Ω to a low-resistance state (e.g., 10^4 Ω for a 10-μA programming current) in less than 100 ns. Cycling appears excellent with projected endurance well beyond 10^{11} cycles.**

***Index Terms*—Electrical switching, nanoscale devices, nanostructured materials, nonvolatile memory, solid-state electrolytes.**

I. Introduction

THE semiconductor industry has acknowledged, via the International Technology Roadmap for Semiconductors,[1] that there will be severe problems with the scaling of solid-state memory as we move toward the end of this decade. Physical size reduction of memory based on charge storage will result in unacceptable state detection or retention and the characteristics of proposed future systems will likely make them unsuitable for most consumer products where cost and power consumption are extremely critical factors. Programmable metallization cell (PMC) memory, which is based on the electrochemical control of nanoscale quantities of metal in thin films of solid electrolyte, shows great promise as a scalable and manufacturable solid-state memory [1], [2].

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[1]The latest version of the International Technology Roadmap for semiconductors is available online. [Online]. Available: http://public.itrs.net

A variety of inorganic and organic materials can conduct ions, but it is the compounds of elements in the column of the periodic table headed by oxygen, the so-called *chalcogens*, that are of particular interest in the context of PMC devices. Certain sulfides and selenides are good solid electrolytes [3], exhibiting ion mobilities as high as 10^{-3} $\mathrm{cm}^2/\mathrm{V}\cdot\mathrm{s}$ and good thermal stability. Nanoscale electrochemical switches have been fabricated using the binary electrolyte Cu_2S, but these have performance limitations, including poor retention, due to the nonideal character of this particular electrolyte [4]. For our nanodevices, we have concentrated on ternary electrolytes formed by the dissolution of silver in a chalcogen-rich germanium–selenide base glass. Standard processing equipment may be utilized and no high-temperature steps are necessary. A silver-containing layer and an inert electrode formed in contact with the electrolyte film creates a device in which information is stored via electrical changes caused by the oxidation of the anode silver and reduction of silver ions in the electrolyte. This occurs at an applied bias as low as a few hundred microvolts and can result in a resistance change of many orders of magnitude for programming currents in the microampere range. A reverse bias of similar magnitude will reverse the process until the excess silver has been removed, thereby erasing the device. Since information is retained via silver electrodeposition rather than charge storage, PMC memory is nonvolatile with excellent retention characteristics. Indeed, our previous research has shown that ten-year state retention is possible even for a write current as low as 2 μA [1].

Our research to date has concentrated on structures with an active device area dimension of 100 nm or larger. This paper discusses new results regarding the basic attributes of sub-100-nm PMC memory devices fabricated using electron beam lithography (EBL). We also used a novel electrolyte formation process for some devices that involves both heat and light to dissolve the silver into the base glass. Attention is given to device fabrication, which uses polymethylmethacrylate layers as the dielectric between the device electrodes, and the nanostructure of the solid electrolyte itself. Electrical characterization includes quasi-static current–voltage and resistance–voltage measurements, as well as single and multiple pulse cycling.

II. Device Fabrication

The PMC device is a simple two-terminal structure, comprising a bottom inert electrode, the solid electrolyte, and an oxidizable metal (Ag) layer, which can also be the top electrode. The electrodes are separated by a dielectric and a through-hole

or "via" in this insulating layer allows the electrolyte to contact the bottom electrode. The diameter D of this via, therefore, defines the active device area as the electrodeposition and, therefore, the resistance reduction will occur in the region of electrolyte between the electrodes. The bottom inert electrode is typically tungsten, although it can be composed of various electrochemically indifferent materials (e.g., platinum). We chose nickel for our nanodevice research due to the ease of processing of this material. The dielectric can also be a variety of materials, but we have concentrated on two in our research to date: SiO_2 for devices with $D > 100$ nm and poly-methylmethacrylate (PMMA) for sub-100-nm devices. The obvious advantage of using PMMA as a nanodevice dielectric is that it can be patterned directly to form the via-holes using standard EBL. The solid electrolyte is typically formed after opening the via by depositing a chalcogenide glass-silver bilayer and then dissolving the Ag into the glass using light at or above room temperature (e.g., around 100 °C). The photodissolved Ag will combine with chalcogen-rich base glasses to form a solid electrolyte with relatively high resistivity, but also with high Ag ion mobility and availability [3], [5]–[7].

For the work reported in this paper, we employed two flows, which we will call process A and process B, to fabricate nanoscale devices with PMMA dielectric and Ni bottom electrodes. In both cases, we started by depositing 100–200 nm of Ni on a 100-nm-thick SiO_2 layer grown on silicon substrates. The Ni was patterned using optical lithography to form the bottom inert electrodes. Immediately following Ni patterning (to avoid significant ambient surface contamination of the Ni), 100 nm of PMMA was deposited by spin casting and baked at 170 °C for 18 h to ensure complete solvent removal.

For process A, the PMMA was exposed at an area dose of 1200 μC/cm^2 using a JEOL 6000 e-beam lithography system to define nanoscale openings aligned to the bottom electrode. Development involved 20 s in a novel developer consisting of 11 : 10 : 1 MIBK : CS : MEK (MIBK is 1 : 3 methyl isobutyl ketone : isopropanol, CS is 3:7 2-ethoxyethanol : methanol, MEK is 2.65 : 7.35 methyl ethyl ketone : ethanol) followed by a 30-s isopropyl alcohol (IPA) rinse. Such conditions lead to high-resolution patterns in the PMMA with steep sidewalls [8]. Immediately following development, approximately 50 nm of base glass was evaporated from a $Ge_{30}Se_{70}$ source under high vacuum (10^{-6} torr) conditions using a resistively heated Knudsen-type cell. This approach helps to ensure that the composition of the deposited film is close to that of the source material. Film composition was assessed using energy dispersive X-ray analysis (EDXA) and the deposited films were apparently slightly lower in Se content than the source (around 2 at.% maximum). Although this could be the case due to re-evaporation of the Se from the deposited film, it is within the measurement error for thin films using this analysis technique. A low deposition rate of 0.03 nm/s was used to facilitate good step coverage/fill in the narrow vias. Immediately following this and without breaking vacuum, 30 nm of Ag for the formation of the solid electrolyte was evaporated. This thickness combination ensures complete saturation of the glass with Ag throughout its depth and leaves a thin residual surface silver layer, approximately 10-nm thick, when the dissolution is driven to completion. For silver diffusion, we used a 0.35-W/cm^2 incandescent (tungsten) broad spectrum source, which provided both heat and light for the dissolution of the silver into the base glass. The exposure was performed under high vacuum to avoid oxidation of the electrolyte layer and lasted 70 min. The approximate steady-state substrate temperature during this step, as measured by a temperature sensor in contact with the sample back, was 70 °C, considerably below the glass transition temperatures of any materials present (note that the T_g of thin-film PMMA is around 120 °C). An additional 100 nm of Ag was evaporated following the dissolution step, again without breaking vacuum, to thicken the top electrode. The samples were then removed from the vacuum system and a layer of optical photoresist was spun on, exposed in a standard optical aligner, and developed to define the electrolyte/top electrode area. The layer was etched in ferric nitrate solution [3-g $Fe(NO_3)_3 \cdot 9H_2O$ in 50-mL deionized water (DI)] and the resist stripped to complete the device structure. Fig. 1 shows field emission scanning electron micrograph cross sections of typical sub-100-nm devices with $D = 75$ nm [see Fig. 1(a)] and $D = 40$ nm [see Fig. 1(b)]. It is clear that the vias in the PMMA in these micrographs have near-vertical sidewalls and the deposition conditions for the electrolyte (labeled $Ag_{33}Ge_{20}Se_{47}$—see Section III) have allowed it to completely fill the narrow openings.

Process B used essentially the same step sequence as process A, the main departures from this being different EBL parameters, Ag dissolution performed using UV light only as in our earlier material and device studies [1], [2], and the use of a gold top electrode to prevent tarnishing of the silver. The PMMA was exposed at 800 μC/cm^2 using the JEOL 6000 EBL system and the patterns were developed as before. Approximately 50 nm of $Ge_{30}Se_{70}$ was evaporated at 0.05 nm/s along with a 30-nm-thick Ag overlayer and the Ag was diffused by exposing it to 405-nm UV radiation at an energy of 1 J/cm^2 to ensure Ag penetration throughout the entire thickness of the electrolyte film. A top electrode bilayer of 80 nm of Ag and 50 nm of Au was then deposited. This stack was then patterned using optical lithography and a combination of sputter etching (to pattern the Au) and wet etching. A field emission scanning electron micrograph cross section of a device produced using this flow with $D = 40$ nm is shown in Fig. 1(c).

III. Electrolyte Nanostructure and Device Switching

Before describing the electrical characteristics of the devices, it is worth considering the composition and nanostructure of the solid electrolyte layer. In general, if we assume that the Ag has a mean coordination of 3, the representation of the composition of ternary Ge–Se–Ag glasses is

$$(Ge_xSe_{1-x})_{1-y}Ag_y = \left(\frac{3y}{2}\right)\left(Ag_{\frac{2}{3}}Se_{\frac{2}{3}}\right) + \left(1-\frac{3_y}{2}\right)(Ge_tSe_{1-t}) \quad (1)$$

where $t = x(1-y)/(1-3y/2)$ is the amount of Ge in the Ge–Se backbone [9]. For $Ge_{30}Se_{70}$, $x = 0.30$, and at saturation

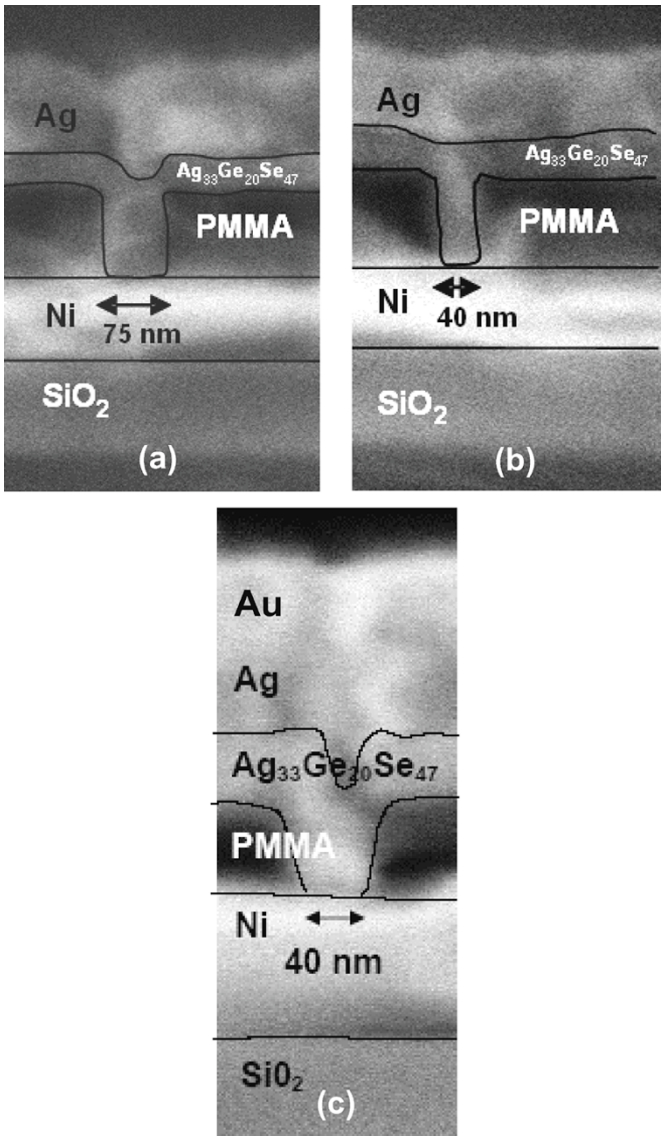

Fig. 1. Electron micrograph cross sections taken by field emission scanning electron microscope of three examples of device structures. The sections were obtained by cleaving the substrate across large arrays of staggered structures so that the break would pass through some of them. (a) Structure with $D = 75$ nm and (b) structure with $D = 40$ nm, both fabricated using process A as described in the text. (c) Structure with $D = 40$ nm fabricated using process B. Charging of the relatively insulating PMMA and solid electrolyte ($Ag_{33}Ge_{20}Se_{47}$) layers leads to poor contrast so the solid lines have been added as a guide to the eye.

$y = 0.333$, we get $t = 0.40$. Put simply, the material consists of Ag_2Se and Ge_2Se_3 in the combination

$$16.7\ Ag_2Se + 10\ Ge_2S_3 = Ag_{33}Ge_{20}Se_{47}. \tag{2}$$

Thus, at saturation, the electrolyte has a Ag_2Se molar fraction of 0.63 (16.7/26.7) and an Ag concentration of 33 at.%. This Ag-saturated composition has been confirmed by us in [5]. We had also previously established that the dissolution of Ag into an Se-rich base glass produces a ternary that is actually a combination of *separate* crystalline Ag_2Se and glassy Ge_2Se_3 phases [10]. In the nanophase separated material, the Ag_2Se phase is dispersed and the Ge-rich insulating phase fills the regions between the crystallites. It is this particular nanostructure

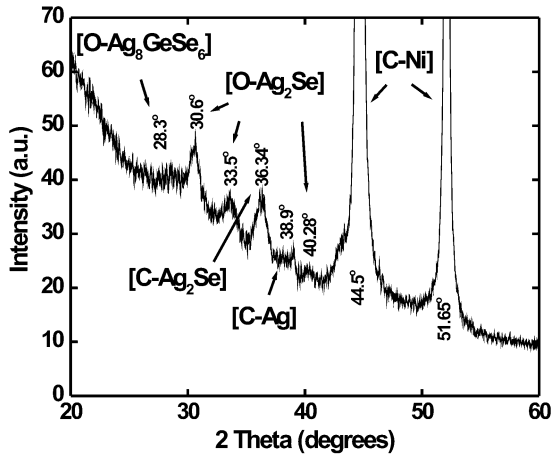

Fig. 2. Results from XRD analysis of the Ag–Ge–Se solid electrolyte film formed on Ni. The peaks were attributed to the presence of labeled materials using the following JCPDS cards: 71-1690 for Ag_8GeSe_6; 20-1063 (peaks at 30.6 and 40.28 for orthorhombic Ag_2Se); 06-0501 (peak at 33.5 for orthorhombic Ag_2Se); 04-0762 (peak at 36.34 for cubic Ag_2Se); 04-0783 (peak at 38.9 for cubic Ag). The strong cubic Ni [C — Ni] peaks at 44.5 and 51.85 (card 87-0712) are from the underlying metal film.

that allows the films to exhibit relatively high resistivity, typically around 100 $\Omega \cdot$ cm or higher, while still possessing good superionic characteristics such as high ion mobility and availability for conduction [3]. Such characteristics are important for PMC device operation, as the electrolyte resistivity coupled with the geometry of the device define the off resistance, and the mobility and availability of Ag ions for electrodeposition within the electrolyte determine the switching characteristics. The distance s between the Ag_2Se phase regions (and, therefore, the thickness of Ge_2Se_3 material between them) can be estimated by assuming that these regions are spherical and uniform in size and dispersion so that

$$s = d\left(F_v^{-\frac{1}{3}} - 1\right) \tag{3}$$

where d is the measured diameter of the crystalline Ag-rich phase and F_v is the volume fraction of this phase. Since the volume fraction of Ag_2Se in $Ag_{33}Ge_{20}Se_{47}$ is 0.57 (for a molar fraction of 0.63), the average spacing between the Ag-rich regions is 0.2 times their diameter.

We have concentrated our current studies on the electrolyte formed using process A (combined heat and light dissolution of the Ag), as we have already extensively investigated the films produced by photodissolution alone (as in process B). We determined the average diameter of the Ag_2Se crystallites in our process A device electrolytes using X-ray diffraction (XRD) techniques on blanket samples of Ag-diffused $Ge_{30}Se_{70}$ on Ni substrates and the results are shown in Fig. 2. XRD conditions were CuK_α emission, 2θ range from 20° to 60° with 0.006° step width, 4.3 s/step. Crystallite size was determined from broadening at half the peak height via the Scherrer formula with $\lambda = 1.5418$ Å for CuK_α emission. The spectrum of Fig. 2 is dominated by the peaks from the underlying cubic Ni [C — Ni] as the ternary film is so thin, but there is strong evidence for the presence of orthorhombic Ag_2Se [O — Ag_2Se], as well as hints of three component orthorhombic Ag_8GeSe_6 and crystalline

c-Ag_2Se and Ag, the latter existing mainly on the surface following the dissolution step from an "excess" Ag source. The appearance of Ag_8GeSe_6 is expected in compositions with 30 at.% or more Ge in the starting glass, especially if heating is involved in the ternary film formation [11]. Analysis of the peaks associated with Ag_2Se suggest that the average diameter of these regions is in the order of 7.5 nm, which means that by (3), they should be separated by 1.5 nm of glassy Ge-rich material.

As previously mentioned, it is this unique nanostructure that gives rise to the characteristics of PMC devices. Although no direct evidence exists for the precise evolution of the electrodeposition process on the nanoscale, it is reasonable to assume that the Ag-rich regions will supply ions for reduction, but that the electrodeposition will occur in the high-resistivity ($> 10_6\ \Omega \cdot$ cm) glassy regions between them where the local electric field is highest [12]. Note that the ions from the Ag-rich regions will be replaced via the ion current from the anode to preserve charge neutrality and electrons will be supplied from the growing electrodeposit, which initiates on (and is, therefore, connected to) the cathode. This will have the effect of bridging the high-resistivity regions with conducting clusters, perhaps containing no more than 100 or so Ag atoms each (the atomic density of pure Ag is 58 atoms/nm^3). In this model, multiple parallel Ag-rich conducting pathways would contain Ag_2Se regions in series with the Ag clusters in the Ge-rich interstices. In the case of electrodeposition that is localized in a relatively small number of bridges, the overall resistance of the conducting pathway will be dominated by the resistivity of the Ag_2Se regions, which is in the order of $2 \times 10^{-3}\ \Omega \cdot$ cm [13]. If this is the case, an on resistance in the order of $10^4\ \Omega$ will require a conducting region of only 20 nm in diameter in our films. The small size of the conducting pathway in comparison to the device area explains why on resistance has been observed to be independent of D, whereas off resistance increases with decreasing area [1]. In the case where the electrodeposit volume dominates, e.g., in a small device, which has had most of its glassy regions bridged, the electrodeposit resistivity will determine the on resistance. Since the electrodeposit resistivity will be more than an order of magnitude smaller than the resistivity of the Ag_2Se regions, the on resistance of even a nanoscale device can be 100 Ω or less.

As in any electrochemical system, the amount of Ag electrodeposited is a function of the magnitude and duration of the Faradaic current. Since the reduction and simultaneous oxidation will only take place when the voltage across the device is above a critical threshold, determined by the materials in the device stack, the on resistance will be determined by the current *limit*. This is so because the decreasing resistance due to the electrodeposition effect increases the current flowing through the device until the current limit is reached, at which point the voltage drop falls to the threshold and the electrodeposition stops. This threshold changes during switching, starting in an unwritten/erased device, in our case, around 200 mV, but dropping to just below 100 mV once the electrodeposition process has been initiated. The on resistance is determined by this latter threshold divided by the programming current limit so that a 10-μA programming current should lead to an on state in the order of $10^4\ \Omega$, but 1 mA would be required for a state nearer to 100 Ω. Thus, in a sub-100-nm device made from a fully saturated electrolyte with a resistivity of 100 $\Omega \cdot$ cm, the off resistance will be in the order of $10^7 - 10^8\ \Omega$ (depending on D and the electrolyte thickness) and the on resistance will be many orders of magnitude below this, depending on the programming current used. One final point linking electrolyte nanostructure to device operation is the effect this will have on the speed of switching. Since the Ag ions are supplied from local Ag_2Se regions, they only have to travel very short distances to join the growing electrodeposit. Considering that Ag ion mobilities in these thin-film materials can be as high as 10^{-3} cm^2/V $\cdot$ s and that the internal electric field can easily be 10^5 V/cm, the electrodeposit growth velocity will be around 1 nm/ns so switching should occur in a few tens of nanoseconds or less for our electrolyte thickness, although the ultimate device speed may be limited by external parasitic effects (see later). We are currently investigating the relationship between switching speed and both electrolyte nanostructure and film thickness and will report on this is in a future publication.

IV. Device Characteristics and Discussion

The quasi-static electrical characteristics of the test devices were obtained by connecting the electrodes, via tungsten probes held in micromanipulators in a vibration and electromagnetic interference isolated probe station, to a semiconductor parameter analyzer (Agilent 4155C). Note that contact to the Ni electrode underlying the dielectric was made by penetrating the relatively soft PMMA with the probe. Voltage double-sweeps were carried out starting at maximum reverse bias (Ni electrode positive, Ag electrode negative), sweeping through zero to an appropriate forward voltage (Ni electrode negative, Ag electrode positive), and sweeping back again through zero to the reverse-bias starting point. This sequence was repeated several dozen times for each device and the acquired data saved in digital format for subsequent plotting. All devices measured were fabricated using process A unless otherwise indicated.

Fig. 3(a) shows a resistance–voltage plot and Fig. 3(b) shows the current–voltage plot for 32 double sweeps on a $D = 75$ nm device. Each sweep runs from -0.5 to $+0.5$ to -0.5 V and the current limit is 10 μA. As expected, the off resistance for forward bias is in the $10^7 - 10^8\ \Omega$ range, although considerable variation is evident from sweep to sweep. This and other variations in the measured data are most likely the result of over-writing due to the large amount of time spent in forward bias following switching because of the slowness of the sweep (several seconds for each sweep direction). Over-writing will result in excess electrodeposited Ag (more than is necessary to switch the device) and this will make the devices more difficult to erase and will lead to varying amounts of Ag in the electrolyte, which will influence the off resistance. Such variation is not evident during faster cycling (see later). The device switches to its low-resistance state around 0.2 V, at which point the current reaches its compliance limit of 10 μA. The current stays at the compliance until the negative-going sweep reaches approximately 0.1 V, at which point the measured on resistance is $10^4\ \Omega$, around 3–4 orders of magnitude lower than the off state. Note that the apparent rise in resistance between 0.1–0.5 V is an artifact of the current compliance control in the measurement

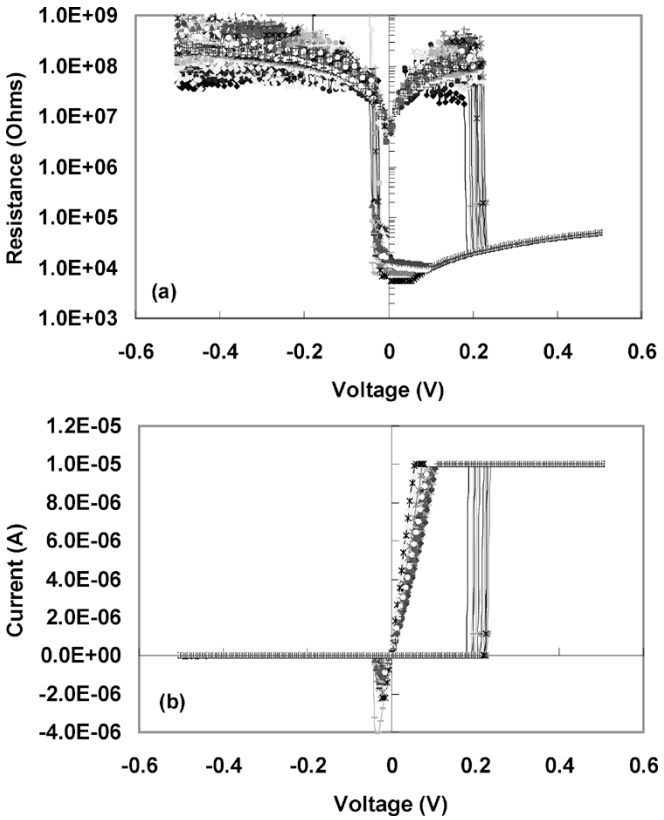

Fig. 3. (a) Resistance–voltage and (b) current–voltage plots from a 75-nm structure fabricated using process A obtained using 32-V sweeps of -0.5 to $+0.5$ to -0.5 V with a 10-μA current limit. The device switches from over 10^7 Ω to its low resistance state of 10^4 Ω around 0.2 V and the conducting pathway breaks at -0.04 V.

instrument. The appearance of the lower threshold following switching is typical of all PMC devices and represents the minimum voltage required for electrodeposition once the process has been initiated and a metal-rich region has formed in the electrolyte (or, more specifically, on the cathode). Electrodeposition within the electrolyte will continue as long as the voltage drop is greater than 0.1 V for this physical configuration. The device transitions to its high-resistance state around -0.04 V, but is not actually erased at this point, as it will switch back to its low-resistance state at an applied bias closer to 0.1 V rather than at the 0.2 V necessary to write a fully erased device. To fully erase the device, the reverse bias must be at least -0.5 V. The sudden increase in resistance at low voltage is due to the initial breaking of the conducting pathway, leading to a device resistance that is dominated by the high resistivity of a small portion of unbridged electrolyte. However, at this point, there is still part of an electrodeposited pathway present, albeit incomplete, and this allows reclosure at the lower threshold. A device that has been fully erased at -0.5 V has very little or none of this residual electrodeposit left and, thus, requires around 0.2 V to rewrite. This is useful in the context of noise immunity in that a "read" voltage of 0.15 V is insufficient to switch a fully erased device, but will reclose a device that was initially on, but had been put in a "soft erase" state by a low (negative) voltage unintended disturb event.

A representative current–voltage plot from a $D = 40$ nm device made using process B [see Fig. 1(c)] under high programming current conditions is presented in Fig. 4. This device was used rather than the 40-nm structure shown in Fig. 1(b), as the high aspect ratio and steep sidewalls of the via created by process A led to poor yield due to small amounts of resist residue being left on the underlying electrode following development. Process B produced less vertical sidewalls and, thus, this via contamination problem was not as prevalent. The plot of Fig. 4 contains six consecutive voltage sweeps from -0.6 to $+0.6$ to -0.6 V, and a 1-mA write current limit was used to drive the device to a low resistance on state around 150 Ω from an off state in the 10^7-Ω range. The write threshold is around 0.2 V as before, but the erase initiation (the point at which the pathway breaks) is around -0.1 V for this more "robust" electrodeposit.

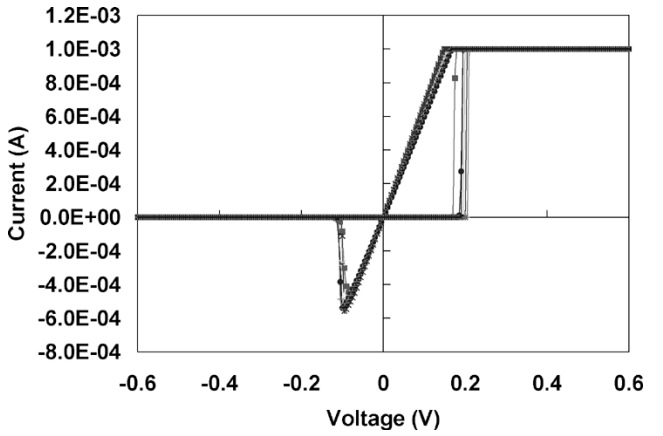

Fig. 4. Current–voltage plot from a 40-nm structure fabricated using process B obtained using six voltage sweeps of -0.6 to $+0.6$ to -0.6 V with a 1-mA current limit. The device switches from over 10^7 Ω to its low resistance state of 100 Ω around 0.2 V and the conducting pathway breaks at -0.1 V.

The above results demonstrate the low voltage and low power switching and large off/on ratios that nanoscale PMC devices are capable of, and our previous work has demonstrated excellent retention characteristics of PMC in general [1]. We will now turn our attention to cycling and endurance of the small-scale devices. The devices are connected via probes as before, but this time, the input signal is supplied by a waveform generator and the output, the voltage drop across a 10^4-Ω resistor in series with the device-under-test, is measured along with the input signal using a digital storage oscilloscope. Unfortunately, this type of setup severely limits the frequency of operation due to the considerable inherent parasitics, especially capacitance that is in the picofarad range (mostly due to the probe pads and connecting cables) and, thus, device maximum speed assessment is not possible. However, it does allow cycling of the devices, although input voltages higher than those used in the quasi-static case are required to overcome the effects of the circuit parasitics. Fig. 5 shows the response of a $D = 75$ nm device (lower waveform), initially in the off state, to an input signal (upper waveform), which goes from -1.3 to $+1.2$ V in 70 ns and 1.6 μs later drops in 70 ns back to -1.3 V. As can be seen in the lower waveform, the device switches to the on state within the rise time of the signal, as indicated by the rise in the test circuit current from its near zero value, although the presence of a parasitic charging current makes the exact point of switching difficult to determine. The transition to the high-resistance state

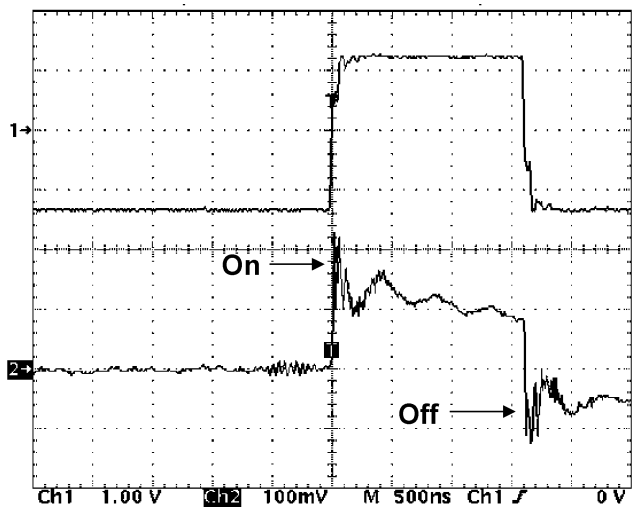

Fig. 5. Digital storage oscilloscope output for the response (lower waveform) of a 75-nm (process A) device to an input signal (upper waveform), which goes from −1.3 to +1.2 V in 70 ns and 1.6 μs later drops in 70 ns back to −1.3 V. The device response/lower waveform is the voltage drop across a 10^4-Ω series resistor and, therefore, is proportional to test circuit current. The horizontal scale is 500 ns per division and the vertical scale is 1 V and 100 mV per division in the upper and lower waveforms, respectively. The device switches to the on and off states within the positive- and negative-going rise times, respectively, of the input signal.

during the negative-going portion of the input signal is also difficult to pinpoint due to the ringing in the output signal, but the sudden drop in current appears to occur within the negative transition of the input. We confirmed that switching was occurring within this time frame by applying single 100-ns-wide pulses from the waveform generator and measuring the resistance using the semiconductor parameter analyzer before and after each pulse. The device resistance did indeed drop from the off level to around 10^4 Ω following the pulse and could be increased again to near 10^7 Ω using a negative-going pulse of the same duration (note that a 10^4-Ω series resistor was used to limit the on current to the 10-μA range).

For cycling, we applied trains of positive (write) pulses of 1.2 V in magnitude and 1.6-μs duration followed by −1.3-V negative (erase) pulses 8.7-μs long. This duty cycle was necessary because of a time constant of several microseconds in the test circuit when the device is in its high-resistance off state. Fig. 6 gives a sequence of output waveforms taken at various numbers of cycles—at the start of the test [see Fig. 6(a)] and at three points in time around 10^{10} cycles apart [see Fig. 6(b)–(d)]. The output waveforms, again the measured voltage across a 10^4-Ω series resistor, show the device switching during the rise in magnitude of the input signal, as determined by the change in test circuit current. The waveform during early cycling appears different from those close to 10^{10} cycles and above [note that the vertical scale on the lower waveform of Fig. 6(a) is 50 mV, whereas it is 100 mV in the lower waveforms of Fig. 6(b)–(d)]. The test circuit current in the on state, averaged over five cycles, is around 8 μA and the maximum averaged current at the off transition is around 3.5 μA. This compares with over 12 and 6 μA for maximum on and off transition currents, respectively, for higher numbers of cycles. This could be due to a "balancing"

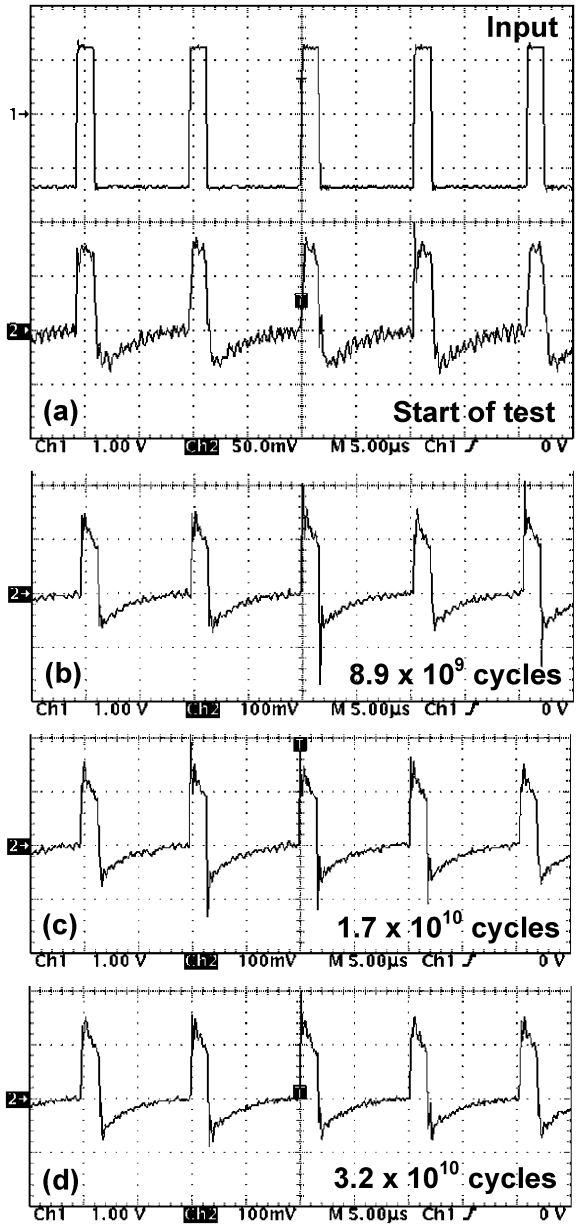

Fig. 6. Digital storage oscilloscope output for 75 nm (process A) device cycling using trains of positive (write) pulses of 1.2-V magnitude and 1.6-μs duration followed by −1.3-V negative (erase) pulses 8.7-μs long. (a)–(d) The output waveforms were taken at various numbers of cycles, as noted in the figure. The horizontal scale is 5 μs per division and the input signal (topmost trace) is common to all output traces (a)–(d) and has a vertical scale of 1 V per division. The vertical scale on the lower trace of (a) is 50 mV, whereas it is 100 mV in the lower traces of (b)–(d).

process, whereby an equilibrium concentration of Ag is reached in the electrolyte during the initial write–erase operations. We are currently investigating this effect, but strongly believe that it can be controlled by optimization of the programming conditions, as well as optimization of device processing. The maximum test circuit current when this quasi-equilibrium is reached is slightly over 12 μA and thereby indicates a total test circuit resistance around 10^5 Ω. Whereas the device on state resistance is relatively easy to obtain from quasi-static voltage sweep or single pulse programming followed by a quasi-static measurement, it is more difficult to precisely determine during cycling

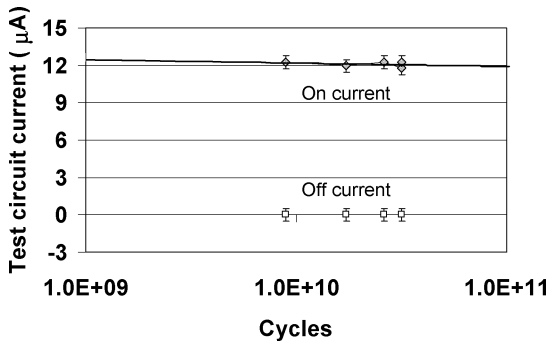

Fig. 7. Test circuit current for the device in the on and off states at various numbers of cycles. The solid line is a logarithmic fit to the data and shows a slight reduction in the test circuit current with a number of cycles.

due to the parasitic effects. However, since there is a known series resistance of $10^4\ \Omega$, we know the device must be below $9 \times 10^4\ \Omega$, which is still 2–3 orders of magnitude below the off state. The transition to the off state on the negative-going edge of the input signal is indicated by the sudden drop in current and subsequent high-frequency ringing. Following this, the voltage and, therefore, the test circuit current decays exponentially from its maximum around 6 μA to zero during the duration of this negative pulse. The slow decay is due to the parasitic capacitance, as mentioned before. Fig. 6(b)–(d) shows little difference in the output waveforms between 8.9×10^9 and 3.2×10^{10} cycles, but careful analysis shows that there actually is a slight drop in the test circuit current with the number of cycles. Fig. 7 shows the average (over five cycles) test circuit on current and minimum off current following decay in the 10^9 to 10^{11} cycles range. The solid line is a logarithmic fit to the on current data (the off current data appears invariant on this scale). This effect could be due to environmental factors such as an increase in series resistance by slow oxidation of the probe to pad contact areas caused by the fact that the devices are cycled on a probe station in uncontrolled laboratory air for hours to days. Fortunately, whatever the origin of this effect, it is slow enough to allow the devices to be taken well beyond 10^{11} write–erase cycles; if the observed logarithmic behavior is maintained, there will only be a 20% decrease in on current at 10^{16} cycles.

V. Summary and Conclusions

We have been successful in fabricating nanoscale PMC devices by utilizing EBL. EBL was used to make sub-100-nm vias in PMMA layers and the solid electrolyte film was formed in these so that the diameter of the via defined the active switching area between the electrodes. The devices were based on an Ag–Ge–Se solid electrolyte created by the photodiffusion, with or without thermal assistance, of an Ag layer into an Se-rich Ge–Se base glass. This leads to a nanophase separated material with a dispersed Ag ion supplying crystalline phase in a high-resistivity Ge-rich continuous phase. The average size of the Ag-rich crystallites in the combined thermal and photodiffusion case, determined using XRD techniques, and the width of the glassy Ge-rich regions between them are 7.5 and 1.5 nm, respectively. This suggests that device scaling to around 10 nm should be possible and research is ongoing to confirm this.

In quasi-static characterization, the devices switched at 0.2 V from an off state in excess of $10^7\ \Omega$ to an on state resistance determined by the write current limit—$10^4\ \Omega$ for 10 μA and 100 Ω for 1 mA. The devices transitioned back to the high off state at or below -0.1 V, becoming fully erased by -0.5 V. Write and erase both occur in less than 100 ns, although the exact switching time of the nanodevices is difficult to determine due to the large parasitic capacitance of the test set up. Cycling endurance of these devices looks promising with little degradation evident up to the low 10^{10} cycle range, although some programming and fabrication optimization are necessary. Extrapolation suggests that cycling to many orders of magnitude greater than this range is possible, making these small devices candidates for low energy dynamic random access memory (DRAM), as well as nonvolatile memory applications.

In memory applications, physical scalability and low-voltage and low-power operation are important, as these characteristics allow high information storage densities. It is clear from the results presented in this paper that switching in the microwatt range is possible and leads to an off/on ratio of more than 10^3, which can be read with simple sense amplifier circuitry, thereby allowing efficient use of chip area for information storage. In addition, the low resistance (in the order of 100 Ω) state is useful for configurable logic applications in which the PMC device would act as a programmable interconnect element in the signal path. In either case, the relative simplicity of the device structure and the techniques used to fabricate them will ensure that manufacturing cost will be reasonable.

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