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Non-Volatile Memory Based on Solid Electrolytes

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Abstract—**Programmable Metallization Cell (PMC) memory utilizes electrochemical control of nanoscale quantities of metal in thin films of solid electrolyte. A silver or copper layer and an inert electrode formed in contact with a Ag^+- or Cu^{2+}-containing electrolyte film creates a device in which information is stored using large non-volatile resistance change caused by the reduction of the metal ions. Key attributes are low voltage, low current, rapid write and erase, good retention and endurance, and the ability for the storage cells to be physically scaled to a few tens of nm. This paper describes the principle of operation of PMC devices and presents representative results from cells with diameters ranging from micron scale to nanoscale dimensions based on Ag-Ge-Se, Ag-Ge-S, and $Cu-WO_3$ solid electrolytes.**

Keywords—electrodeposition; non-volatile memory; resistance change; solid electrolyte.

I. INTRODUCTION

The semiconductor industry has acknowledged, via the International Technology Roadmap for Semiconductors [1], that there will be severe problems with the scaling of solid state memory as we move toward the end of this decade. Physical size reduction of memory based on charge storage will result in unacceptable retention or state detection characteristics and the voltage, power, and cost requirements of upcoming memory applications, especially those in portable or "untethered" systems, make many other approaches to solid state data storage undesirable. Programmable Metallization Cell (PMC) memory, which utilizes electrochemical control of nanoscale quantities of metal in thin films of solid electrolyte, shows great promise as a future solid state memory [2,3]. Key attributes are low voltage and current operation, excellent scalability, and a simple fabrication sequence. Device formation involves the dissolution of silver or copper in a chalcogenide (e.g., germanium selenide, germanium sulfide) or oxide (e.g., tungsten oxide) base glass to create a solid electrolyte. A silver- or copper-containing layer and an inert electrode formed in contact with the electrolyte film creates a device in which information is stored via electrical changes caused by the oxidation of the silver or copper metal and reduction of silver or copper ions in the electrolyte. This occurs at an applied bias as low as a few hundred mV and can result in a resistance change of many orders of magnitude within a few tens of nanoseconds even for currents in the μA range. A reverse bias of the same magnitude will reverse the process until the electrodeposited metal has been removed, thereby erasing the device. Since information is retained via

metal atom electrodeposition rather than charge storage, PMC memory has excellent retention characteristics.

This paper reviews the basic electrochemistry that enables PMC memory device operation and gives examples of measured characteristics for devices with diameters ranging from 1 μm to 40 nm which utilize both chalcogenide- and oxide-based solid electrolytes.

II. PRINCIPLE OF OPERATION

Solid electrolytes are somewhat analogous to liquid electrolytes in that ions in the material can be plentiful and highly mobile. However, in solid electrolytes containing metal ions, only the positively charged ions are mobile and the negatively charged counter-ions are fixed in the solid. If an anode containing oxidizable metal and an electrochemically inert cathode are formed in contact with a layer of solid electrolyte, an applied voltage as low as a few hundred mV will reduce ions to form metal atoms at the cathode and put ions into the electrolyte via oxidation at the anode. Charge neutrality will be maintained if oxidation and reduction are in balance and so a source of oxidizable metal is required to sustain ion reduction in the electrolyte, otherwise the build-up of charge would halt the *electrodeposition* process. Note that given this condition, electrodeposition of metal in the electrolyte cannot proceed if the oxidizable electrode is made negative with respect to the inert electrode ("reverse bias"). Also, the flow of ions in forward bias will cease if the potential across the structure drops below that necessary to stimulate electrodeposition or if the supply of oxidizable metal becomes exhausted.

The solid electrolyte is simple to make. Many inorganic and organic (including polymeric) materials can conduct ions but it is the compounds of elements in the column of the Periodic Table headed by oxygen, the so-called *chalcogens*, that are of particular interest in the context of PMC devices. We typically focus on those which make thermally stable compounds - oxygen (O), sulfur (S), and selenium (Se). Combining these with copper (Cu) or silver (Ag) yields binary electrolytes like Ag_2Se or Cu_2S [4]. Alternatively, a transition metal such as tungsten (W) can be reacted with oxygen to form a base glass for an electrolyte [5]. If the resulting tungsten oxide is sufficiently porous and in the trioxide form (WO_3), silver or copper ions will be mobile within the material and can form electrodeposits. Yet another approach is to combine chalcogens with other elements such as germanium (Ge) to create a base glass into which we can dissolve Cu or Ag. An example of such a ternary electrolyte is 33 atomic %

Ag dissolved in $Ge_{30}Se_{70}$, i.e., $Ag_{33}Ge_{20}Se_{47}$. This takes the form of a continuous glassy Ge_2Se_3 backbone and a dispersed nanoscale Ag_2Se phase [6,7] which is *superionic* and allows the electrolyte to exhibit superionic qualities The distinctive nanostructure of this material and its sulfide counterpart [8] leads to ideal characteristics in the context of switching devices. The metal-rich phase is both an ion and an electron conductor but the backbone material that separates each of these conducting regions is a good dielectric so the overall resistance of the material prior to electrodeposition is high.

The solid electrolyte can be made to contain ions throughout its thickness. The ions nearest the electron-supplying cathode will move to its surface and be reduced first. The non-uniformities in the ion distribution and in the nano-topography of the electrode will promote localized deposition or nucleation. Even if multiple nuclei are formed, the one with the highest field and best ion supply will be favored for subsequent growth, extending out from the cathode as a single metallic nanowire. The electrodeposition of metal on the cathode does not mean that an ion entering from the oxidizable anode has to travel the entire length of the structure to replace a reduced ion. The ion closest to the reduction zone will move to the vacated negative site on the hosting material and those upstream will do likewise, each filling the vacated site of the one downstream, until the last vacated space closest to the anode is filled by the incoming ion; the ion current is actually a *coordinated motion* of ions. The electrodeposition of metal on the cathode physically extends the electrode into the electrolyte. This physical intrusion is possible in solid electrolytes, particularly if they are glassy in nature and can accommodate the growing electrodeposit in their void-rich, semi-flexible structure. Since the electrodeposit is connected to the cathode, it can supply electrons for subsequent ion reduction. So the advancing electrodeposit will harvest ions from the electrolyte, plating them onto its surface to extend itself forward. This means that the growing electrodeposit is always adjacent to a significant source of ions in a electrolyte that contains many tens of atomic percent of metal ions and so the average distance each ion has to travel in order to be reduced is a few nm at most. The resistivity of the electrodeposit is many orders of magnitude lower than that of the surrounding electrolyte so once the electrodeposit has grown from the cathode to the anode, the resistance of the structure drops considerably. The decreasing resistance due to the electrodeposition effect increases the current flowing through the device until the current limit of the source is reached. At this point, the voltage drop falls to the threshold for electrodeposition and the process stops, yielding the final resistance of the structure.

The electrodeposition process is reversible by changing the polarity of the applied bias and much the same rules that govern growth apply. If the electrodeposit is made positive with respect to the original oxidizable electrode, it becomes the new anode and will dissolve via oxidation. During the dissolution of the conducting pathway, the balance is maintained by electrodeposition of metal back onto the place where the excess metal for the electrodeposition came from in the first place. Note that the original growth process will have left a low density region at this electrode and this "free volume" will favor redeposition without extended growth back into the electrolyte. Once the electrodeposit has been completely dissolved, the process self-terminates. It is important to note that it is the asymmetry of the structure that allows cycling of the devices between a high resistance off state and a low resistance on state and thereby allows them to operate as switches and memory elements.

III. DEVICE FABRICATION

A. Chalcogenide-based electrolytes

The PMC structure typically comprises a bottom inert electrode, the solid electrolyte, and an oxidizable metal layer which can also act as the top electrode. The electrodes are separated by a dielectric and a through hole or via in this insulating layer defines the electrolyte area that contacts the bottom electrode. The diameter, D, of this via delineates the active device area as the electrodeposition and the consequent resistance reduction will occur in the region of electrolyte between the electrodes.

In our chalcogenide-based devices, the bottom inert electrode is usually tungsten although it can be composed of various electrochemically indifferent materials such as nickel (Ni), which we used in our nanodevice work [3]. The dielectric can also be a variety of materials but we have concentrated on two in our work to date: deposited silicon dioxide for devices with D > 100 nm and spin-cast poly-methylmethacrylate (PMMA) for sub-100 nm devices. The obvious advantage of using PMMA as a nanodevice dielectric is that it can be patterned directly to form the via holes using standard electron beam lithography (EBL) [3].

The chalcogenide electrolyte is typically formed after via etch by depositing a 50 nm thick chalcogen-rich Ge_xSe_{1-x} or Ge_xS_{1-x} (x < 0.33) base glass layer followed by a 25 nm thick layer of Ag, both by physical vapor deposition (PVD). The Ag is then dissolved into the base glass using one of two processes; (1) exposure to ultraviolet light, 405 nm, 1 J/cm^2, at room temperature, or (2) exposure to a 0.35 W/cm^2 incandescent (tungsten) broad spectrum source under high vacuum for several tens of minutes to provide both heat and light (the approximate steady state substrate temperature is 70°C). Process 1 is used for devices with D > 100 nm as it can be used to produce an electrolyte which has a thin sub-saturated and therefore high resistivity (> 10^6 Ω.cm) layer above the cathode, thereby allowing a high off resistance even in large diameter structures. Process 2 is used in nanodevice fabrication as it promotes complete Ag saturation of the electrolyte throughout its thickness but the small diameter results in a high off resistance even for a saturated electrolyte resistivity around 100 Ω.cm. Following dissolution, an additional 50 nm of Ag is added to ensure a source for the electrodeposition and this is capped with the top electrode layer (this can also be a variety of metals but we tend to use gold (Au) to prevent tarnishing of the silver during testing). Figure 1 illustrates the basic structure of a PMC memory test device. This particular device was fabricated using electron-beam exposure of a PMMA dielectric film on Ni and utilizes a Ag-Ge-Se electrolyte capped with Au.

B. Oxide-based electrolytes

PMC devices based on WO_3 are also extremely simple to make. A 100 nm thick tungsten layer is deposited by chemical
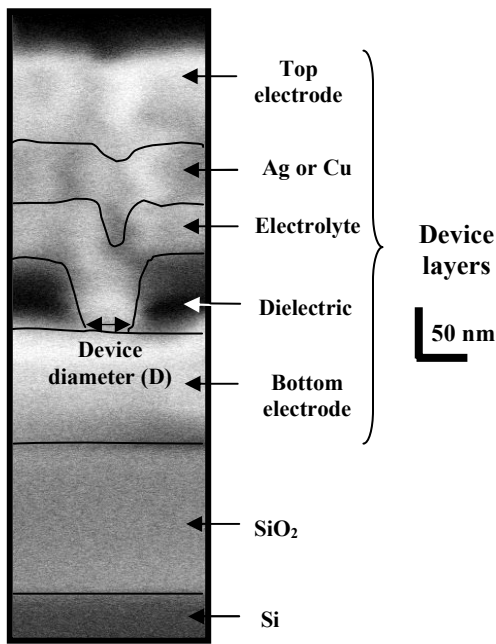
Figure 1. Field emission scanning electron microscope photographic cross section of a PMC structure showing the main layers. This device was formed in a 40 nm via (at the base) in a PMMA dielectric and consists of a Ni bottom electrode, Ag-Ge-Se electrolyte, and a Ag anode and Au top electrode. A 50 nm horizontal and vertical size bar is shown to the right of the micrograph and the solid lines at the layer interfaces have been added for clarity.

vapor deposition (CVD) on silicon dioxide grown on silicon substrates and covered with 100 nm of silicon dioxide by CVD. Vias are defined in this deposited dielectric using optical lithography and dry etching. The exposed tungsten in the holes is oxidized by plasma oxidation using a nitrous oxide (N_2O, 20 sccm with 1000 sccm of He carrier gas) glow discharge at an RF power of 250 W and a substrate heater temperature of 300°C for 10 minutes in a plasma processing system. This creates a WO_3 base glass layer on the W electrode that is approximately 3 nm thick. Ag or Cu layers, 50 nm thick, are then deposited by high vacuum thermal evaporation and diffusion into the oxide is achieved by illumination with light of 405 nm [9]. The top Ag or Cu electrode is then deposited by high vacuum thermal evaporation and patterned by optical lithography and lift-off. Note that in this case, the WO_3 electrolyte is present only at the base of the via.

IV.   RESULTS AND DISCUSSION

A.   Chalcogenide-based devices

Results from the electrical characterization of a variety of PMC devices are presented and discussed in this section. Quasi-static electrical characteristics of the test devices were obtained by connecting the electrodes, via tungsten probes held in micromanipulators in a vibration- and electromagnetic interference-isolated probe station, to a semiconductor parameter analyzer (Agilent 4155C). Voltage double-sweeps were carried out starting at maximum reverse bias (W or Ni electrode positive, Ag/Au electrode negative), sweeping through zero to an appropriate forward voltage (W or Ni

electrode negative, Ag/Au electrode positive), and sweeping back again through zero to the reverse bias starting point. The acquired data was saved in digital format for subsequent plotting and analysis.

Figure 2(a) shows a representative single current-voltage plot and Figure 2(b) a single resistance-voltage plot for a Ag-Ge-Se solid electrolyte device with D = 0.24 μm. The programming current limit was 1 μA and the voltage sweep was -1.0 V to +0.5 V to -1.0 V. The device switches at 0.24 V from an off-state resistance, R_{off}, close to 10^{10} Ω to an on-state resistance, R_{on}, more than 4 orders of magnitude lower for this programming current. Note that the apparent rise in resistance following switching is caused by the current limit (compliance) control in the measurement instrument. Once electrodeposition is initiated, the threshold for further electrodeposition is decreased. This is evident by the presence of a lower voltage, in this case 0.14 V, at which the current drops below compliance on the negative-going sweep (see the right side of the plot of Figure 2(a)). The appearance of a reduced threshold is typical of all PMC devices, including those with oxide electrolytes (described later) and represents the minimum voltage required for electrodeposition once a metal-rich region has been formed in the electrolyte.
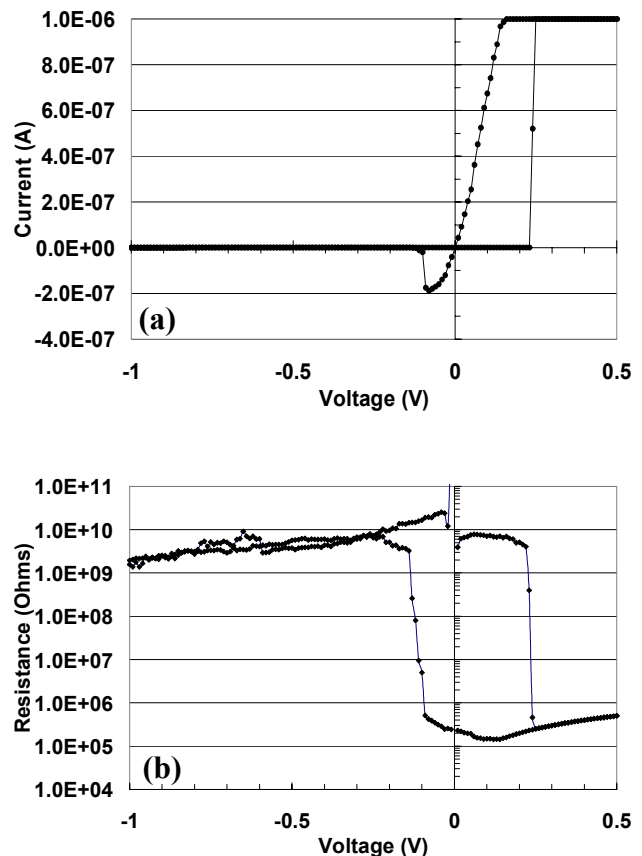

Figure 2. (a) Current–voltage plot of a device with a Ag-Ge-Se electrolyte (D = 0.24 μm) using a 1 μA current limit. Voltage sweep is -1.0 V to +0.5 V to -1.0 V. Write threshold is approximately 0.24 V. (b) Resistance-voltage plot of the same device. Off-state resistance is in excess of 1 GΩ over the voltage range shown and the on-state resistance is over 4 orders of magnitude lower.

The on-state resistance minimum, in this case $1.4 \times 10^5 \, \Omega$, is defined by the lower threshold and the programming current limit (see later in this section). The slight rise in resistance below 0.14 V indicates a non-ohmic component in the conducting pathway. The device transitions to a high resistance state around -0.1 V and this characteristic is assumed to be due to the initial breaking of the electrodeposited pathway, however, there will still be a partial Ag-rich pathway in the electrolyte at this point. This can be confirmed by the fact that a device that is not swept beyond -0.1 V will re-write around 0.13 to 0.15 V rather than the 0.24 to 0.26 V it takes to write a new or fully erased device, the latter having been swept to -0.3 V or more. Continuing the negative sweep, the off resistance remains above $10^9 \, \Omega$ as the voltage is swept out to -1.0 V but there is an exponential decrease in resistance/rise in current due to the (electron) leakage current in the high resistivity electrolyte. The leakage current is approximately 0.5 nA at -1.0 V.

Figure 3 shows the dependence of R_{on} on the programming current limit, I_{prog}, in the range 1 to 10 µA. R_{on} is related to I_{prog} via the relationship

$$R_{on} = 0.14/I_{prog}. \qquad (1)$$

This is explained by the fact that as long as sufficient potential difference is maintained for the situation where electrodeposition is already underway, in this case 0.14 V, the reduction of silver ions will persist and the resistance of the conducting bridge will continue to fall even after it has formed. However, if the external current source is limited, once the resistance falls to a point where the voltage drop is no longer sufficient to support reduction, the electrodeposition process ceases and the resistance between the electrodes remains constant. The minimum "closed" resistance in ohms is therefore given approximately by the minimum potential to sustain electrodeposition in volts divided by the current limit of the external supply in amps. For the devices under study here, a 1 µA current limit will therefore give an on resistance of 140 kΩ whereas a 1 mA current will yield an on state closer to 140Ω (see later).

The resistance change is quite stable, as illustrated in Figure 4, which gives on resistance vs. time averaged from two Ag-Ge-Se electrolyte devices, D = 1 µm, programmed with a 2µA

Figure 4. Average on-state resistance vs. time for two Ag-Ge-Se electrolyte devices (D = 1 µm) programmed using a 2 µA current limit. Off-state resistance for these devices was around $10^9 \, \Omega$.

current limit. Off-state resistance for these devices was in the order of $10^9 \, \Omega$. An upward drift in resistance with time is evident, reaching an extrapolated value near $5 \times 10^7 \, \Omega$ at 10 years. The origin of this resistance increase is most likely the slow diffusion of metallic Ag from the electrodeposition pathway into local defects in the electrolyte. The off/on ratio of greater than 10x at 10 years is encouraging with such a low programming current but the relatively high value of R_{on} would lead to slow read times. Higher programming currents produce more impressive results. Figure 5 uses extrapolated data (1 month actual test time) from 1 µm devices programmed using 1 to 30 µA to illustrate R_{on} dependence on write current following (a) 10 years at room temperature and (b) 10 years at 70°C. This extrapolated data suggests that a write current in excess of 30 µA is required to maintain sub-100 kΩ R_{on} after 10 years at 70°C. Note that the activation energy extracted from this analysis was approximately 0.2 eV.

Germanium sulfide-based devices have very similar electrical characteristics to their selenide counterparts but the Ag-Ge-S electrolytes are able to withstand higher process temperatures (mid-400°C range) than the Ag-Ge-Se materials (mid-200°C range) without modification. Figure 6(a) shows a current-voltage plot and Figure 6(b) a resistance-voltage plot for a Ag-Ge-S electrolyte device, D = 0.24 µm, that has been annealed in dry N_2 at 370 °C for 15 mins. The programming
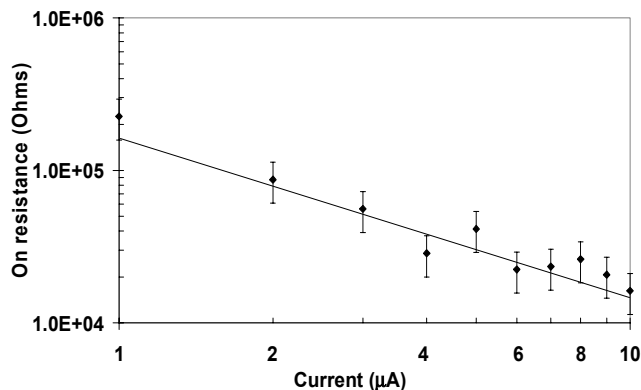

Figure 3. On-state resistance vs. programming current for a device with a W bottom electrode and Ag-Ge-Se electrolyte (D = 1 µm). The resistance value in Ω is approximately 0.14 divided by the current in A (solid line).

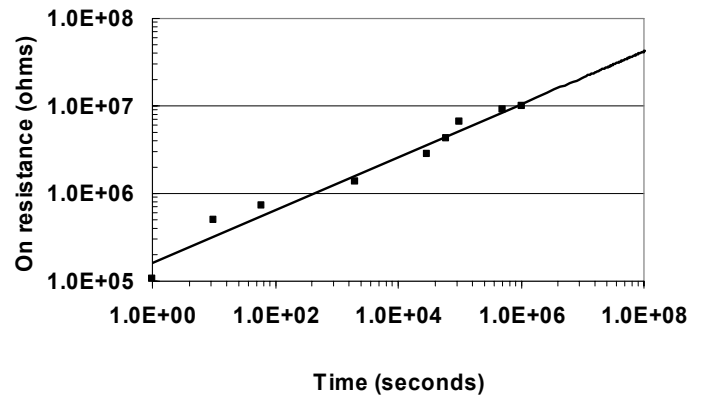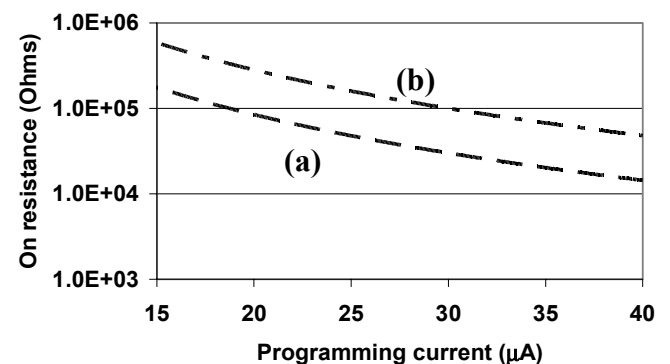Figure 5. Extrapolated on-state resistance after 10 years at (a) room temperature and (b) 70 °C for Ag-Ge-Se electrolyte devices (D = 1 µm).

current limit was 1 μA and the voltage sweep was -1.0 V to +0.5 V to -1.0 V. The device switches at 0.38 V from an off state resistance, R_{off}, above 10^{10} Ω to an on resistance state, R_{on}, more than 5 orders of magnitude lower. It is expected that sulfide-based devices will have an off resistance around 50 times higher than a similarly fabricated selenide device due to the higher resistivity of this electrolyte [10] but the rise in switching threshold from around 0.26 V before anneal to 0.38 V is a consequence of the heating process. This is thought to be due to top electrode damage in these unpassivated devices as higher annealing temperatures cause obvious electrode failure while causing little change in the sulfide-based electrolyte. This is currently under investigation by our group.

B. Nanoscale devices

A representative current-voltage plot from a nanoscale Ni cathode Ag-Ge-Se device, D = 40 nm, under high programming current conditions is presented in Figure 7. This plot contains 6 consecutive voltage sweeps from -0.6 to +0.6 to -0.6 V and a 1 mA write current limit was used to drive the device to a low resistance on state around 150 Ω from an off state in the 10^7 Ω range. The write threshold is 0.2 V, which is typical for Ni cathode devices, and the threshold after initiation

(a)

(b)

Figure 6. (a) Current–voltage plot of a device with a Ag-Ge-S electrolyte (D = 0.24 μm) following a 15 minute anneal at 370 °C in an inert ambient. Current limit was 1 μA and the voltage sweep was -1.0 V to +0.5 V to -1.0 V. Write threshold is approximately 0.38 V. (b) Resistance-voltage plot of the same device. Off-state resistance is well in excess of 10 GΩ over the voltage range shown and the on-state resistance is over 5 orders of magnitude lower.
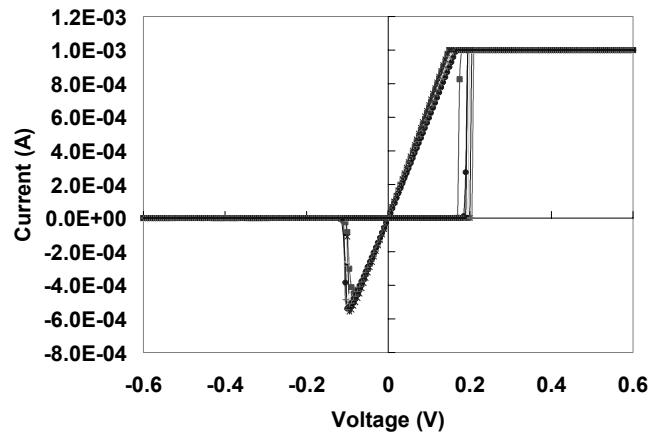
Figure 7. Current-voltage plot from a 40 nm Ag-Ge-Se device obtained using 6 voltage sweeps of -0.6 to +0.6 to -0.6 V with a 1 mA current limit. The device switches from over 10^7 Ω to its low resistance state of 150 Ω at 0.2 V.

is 0.15 V. The pathway breaking occurs at -0.1 V as before, even for this "robust" electrodeposit. The use of such a high programming current was based on our desire to demonstrate that even nanoscale devices can be driven to a resistance that is low enough to allow them to be used as switching (as well as memory) elements in programmable logic applications.

We will now turn our attention to cycling and endurance of scaled structures. The devices are connected via probes as before but this time the input signal is supplied by a waveform generator and the output, the voltage drop across a 10^4 Ω resistor in series with the device under test, is measured along with the input signal using a digital storage oscilloscope. Unfortunately, this type of set up severely limits the frequency of operation due to the considerable inherent parasitics, especially capacitance which is in the pF range (mostly due to the probe pads and connections), and so device maximum speed assessment is not possible and input voltages higher than those used in the quasi-static case are required.

Trains of positive (write) pulses of 1.2 V in magnitude and 1.6 μsec duration followed by -1.3 V negative (erase) pulses 8.7 μsec long, as shown in Figure 8(a), were used to cycle the devices. This duty cycle was necessary because of a time constant of several μsec in the test circuit when the device is in its high resistance off state. Figure 8 also gives two output waveforms taken at the start of the test, 8(b), and at 3.2×10^{10} cycles, 8(c). The waveform during early cycling appears different from those around 10^{10} cycles (note that the vertical scale in Figure 8(b) is 50 mV whereas it is 100 mV in Figure 8(c)). The peak test circuit current in the on state, averaged over 5 cycles, is approximately 8 μA at the start, compared with over 12 μA for higher numbers of cycles. This could be due to a "balancing" process, whereby an equilibrium concentration of Ag is reached in the electrolyte during the initial write-erase operations. We are currently investigating this effect but strongly believe that it can be controlled by optimization of the programming conditions, as well as optimization of device processing.

The maximum test circuit current when the quasi-equilibrium condition is reached is slightly over 12 μA and thereby indicates a total test circuit resistance around 10^5 Ω. Whereas the device on state resistance is relatively easy to

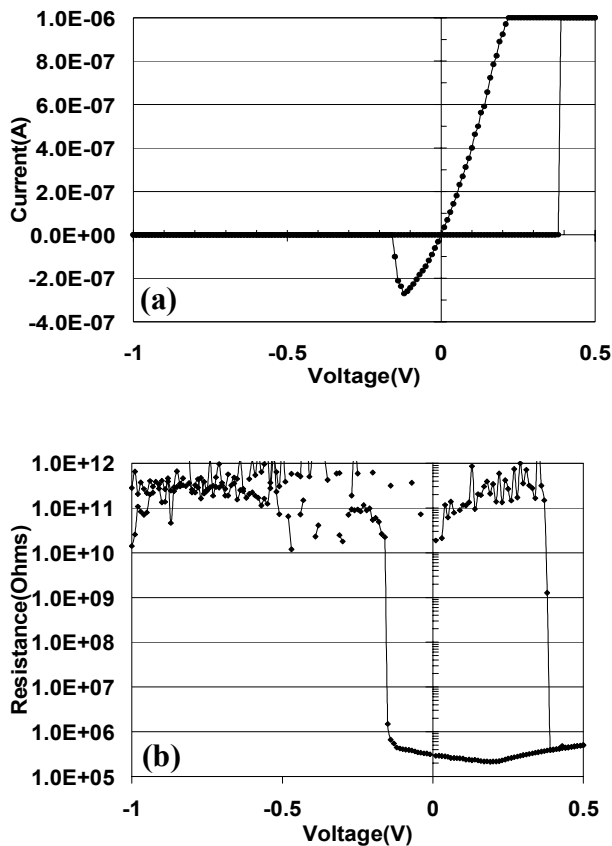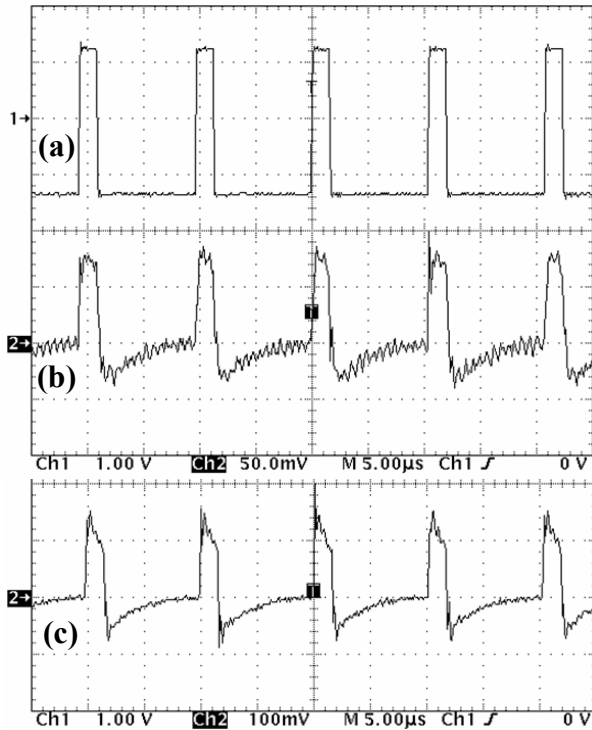Figure 8. Digital storage oscilloscope output for a Ag-Ge-Se device, D = 75 nm, during cycling using trains of positive (write) pulses of 1.2 V in magnitude and 1.6 µsec duration followed by -1.3 V negative (erase) pulses 8.7 µsec long. The horizontal scale is 5 µsec per division and the input signal (a) is common to the two lower output traces and has a vertical scale of 1 V per division. The output waveforms are the voltage drop across a $10^4 \ \Omega$ series resistor and therefore are proportional to test circuit current. These were taken at the start of the test (b) and after 3.2×10^{10} cycles (c). The vertical scale in (b) is 50 mV whereas it is 100 mV in (c).

obtain from quasi-static voltage sweep or single pulse programming followed by a quasi-static measurement, it is more difficult to determine precisely during cycling due to the parasitic effects. However, since there is a $10^4 \ \Omega$ resistor in the current path, we know the device must be below $9 \times 10^4 \ \Omega$ which is still 2 to 3 orders of magnitude below the off state. The transition to the off state on the negative going edge of the input signal is indicated by the sudden drop in current and subsequent high frequency ringing. Following this, the voltage and therefore the test circuit current decays exponentially from its maximum around 6 µA to zero during the duration of this negative pulse. The slow voltage decay is due to the parasitic capacitance, as mentioned before.

Analysis of the test circuit current during cycling at various points between 10^9 and 10^{11} cycles shows that there may be a slight decrease in this parameter with the number of cycles. Figure 9 shows the average (over 5 cycles) test circuit on current and minimum off current in the 10^9 to 10^{11} cycles range. The solid line is a logarithmic fit to the on current data (the off current data appears invariant on this scale). The apparent slight reduction in on current with cycle number could be due to environmental factors such as an increase in series resistance by slow oxidation of the probe to pad contact areas caused by the fact that the devices are cycled on a probe station in laboratory air with some humidity for hours to days.
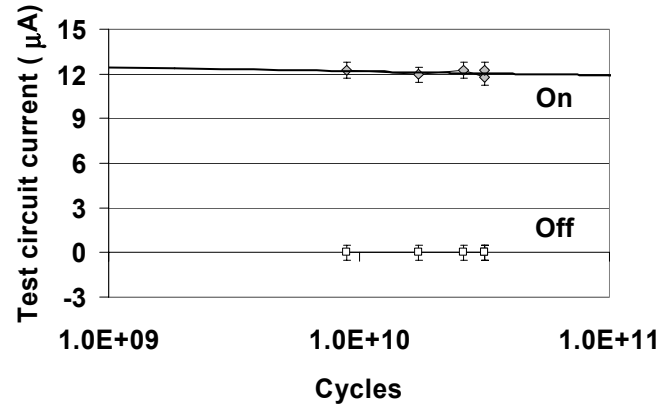

Figure 9. Test circuit current for the device of Figure 8 in the on and off state at various numbers of cycles. The solid line is a logarithmic fit to the data.

Fortunately, whatever the origin of this effect, it is gradual enough to allow the devices to be taken well beyond 10^{11} write-erase cycles. Indeed, if the observed decline in on-state current is maintained, extrapolation of the logarithmic plot suggests that there will only be a 20% decrease in on current at 10^{16} cycles.

To illustrate device switching during each cycle, Figure 10 shows the response (lower waveform) of a Ag-Ge-Se, D = 75 nm device, initially in the off state, to an input signal (upper waveform) which goes from -1.3 V to +1.2 V in 70 nsec and 1.6 µsec later drops in 70 nsec back to -1.3 V. As can be seen in the lower waveform, the device switches to the on state within the time the input signal takes to rise from 0 V to its final value, approximately 35 nsec, as indicated by the rise in test circuit current from its near zero value, although the presence of parasitic charging current makes the exact point of switching difficult to determine. The transition to the high resistance state during the negative going portion of the input signal is also difficult to pinpoint due to ringing in the output
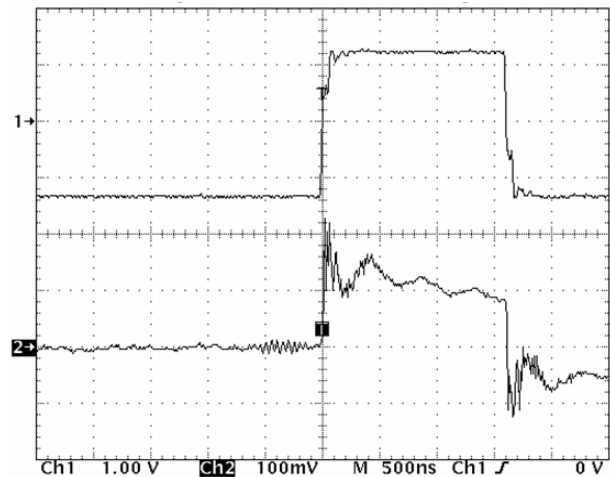

Figure 10. Digital storage oscilloscope output for the response (lower waveform) of the device of Figure 8 to an input signal (upper waveform) which goes from -1.3 V to +1.2 V in 70 nsec and 1.6 µsec later drops in 70 nsec back to -1.3 V. The horizontal scale is 500 nsec per division and the vertical scale is 1 V and 100 mV per division in the upper and lower waveforms respectively.

signal but the drop in current occurs within the 35 nsec transition of the input. Fast switching was confirmed by applying single 100 nsec pulses and measuring the resistance before and after each pulse. The 75 nm device resistance did indeed drop from the off level to around 10^4 Ω following the pulse and could be increased again to near 10^7 Ω using a negative going pulse of the same duration (note that a 10^4 Ω series resistor was used to limit the on current to the 10 µA range). Single 25 nsec pulses have also been used on larger devices with much the same effect. We expect the intrinsic switching time of these devices to be considerably smaller. For thin electrolyte films between the electrodes, most of the applied voltage will be dropped across the polarized region where electrodeposition occurs (typically a few tens of nanometers thick) and the field will therefore be in the order of 10^5 V/cm. Ion mobility at such fields in the best solid electrolytes can be as high as 10^{-3} cm^2/V.s and these figures lead to an electrodeposit growth rate of at least 1 nm/ns. This suggests that an electrolyte with a less than 10 nm of bridgeable path should switch in less than 10 nsec.

C. Oxide-based devices

The quasi-static characteristics of tungsten oxide test devices were obtained as before using the probe station and the semiconductor parameter analyzer. Voltage double-sweeps were carried out starting at maximum reverse bias (tungsten electrode positive, oxidizable electrode negative), sweeping to the maximum forward voltage (tungsten electrode negative, oxidizable electrode positive), and sweeping back again to the reverse bias starting point. Figure 11 shows a representative current-voltage plot for a 0.3 µm diameter PMC device with Ag/plasma-grown WO$_3$ electrolyte and Ag oxidizable electrode. The sweep runs from -0.75 V to +1.0 V to -0.75 V and the current limit is 1 µA. The maximum off resistance is in excess of 10^{10} Ω and the device switches to its low resistance state at 0.7 V, at which point the current reaches its compliance limit of 1 µA. The current stays at the compliance until the negative-going sweep reaches the minimum threshold for electrodeposition of 0.25 V, at which point the measured on resistance is 2.5 x 10^5 Ω, five orders of magnitude lower than the maximum off state. Note that the

low resistance on state shows some non-ohmic character near the origin of the I-V plot (much more so than in the case of the chalcogenide-based devices). The device transitions to its high resistance state at -0.15 V, although it does not reach maximum off resistance until -0.5 V. The sudden increase in resistance at low voltage is again most likely due to the initial breaking of the conducting pathway, leading to a device resistance that is dominated by the high resistance of a portion of now unbridged electrolyte. The subsequent resistance rise is a result of the removal by oxidation of the remaining electrodeposited silver. We also observed a drop in off state resistance for increasing voltage magnitude in either direction and attribute this to the leakage (tunneling) current in the thin electrolyte.

Figure 12 shows the resistance-voltage plot for a 1 µm diameter PMC device with Cu/plasma-grown WO$_3$ electrolyte and Cu oxidizable electrode. Three consecutive sweeps are shown for a current limit of 0.5 µA. The maximum off resistance for the first sweep is well in excess of 10^{10} Ω and the transition to the low resistance state occurs at 0.9 V. However, it is clear that the first sweep is different from the following two in that the off resistance is lower by an order of magnitude and the initial switching threshold moves closer to 0.7 V in the latter cycles. This effect was not as obvious in the Ag-doped samples and we assume it is related to the oxidation of copper in the diffusion process [9]. We believe that the first sweep injects Cu from the anode to bring the material nearer Cu ion saturation, hence the lower off resistance and lower write threshold for the following sweeps. Once again, the apparent drop in the resistance in the 1.0 to 0.25 V range is due to the way that the measurement system controls the current at the limit. The post-electrodeposition threshold, as determined by the point at which the on resistance reaches its minimum value, is 0.20 V for the first sweep and 0.25 V for sweeps 2 and 3. The minimum on resistance is 4 x 10^5 Ω for the first sweep and 5 x 10^5 Ω for subsequent sweeps, some three to four orders of magnitude lower than the off resistance for the small programming current of 0.5 µA. The erase transition voltage varies from 0.2 to 0.3 V in this device with full erase occurring at -0.5 V as in the Ag case.
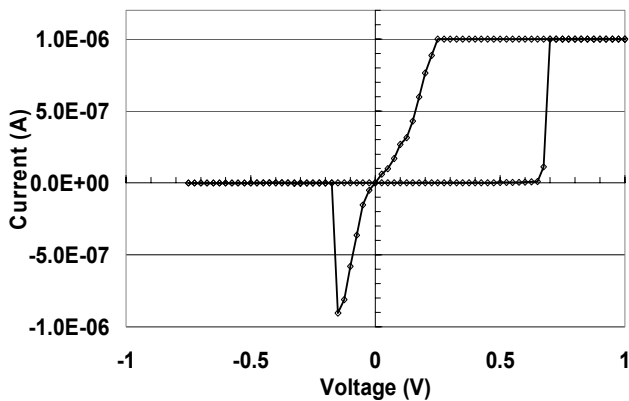

Figure 11. Current–voltage plot of a 0.3 µm diameter PMC device with Ag/plasma-grown WO$_3$ electrolyte and Ag oxidizable electrode. Compliance current was 1 µA. The device switches from over 10^{10} Ω to an on state over five orders of magnitude lower at 0.7 V.
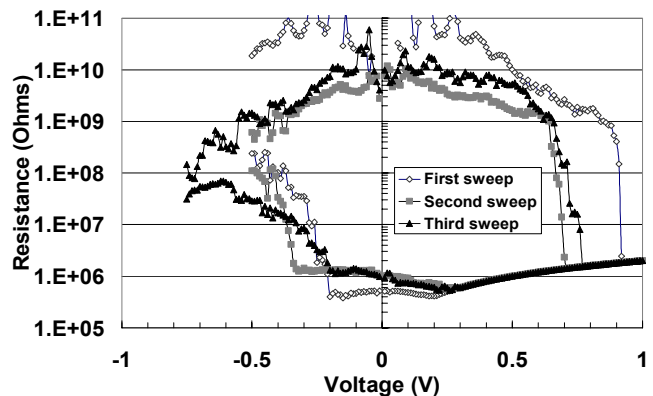

Figure 12. Resistance-voltage plot (3 sweeps) of a 1 µm diameter PMC device with Cu/plasma-grown WO$_3$ electrolyte and Cu oxidizable electrode. The programming current limit was 0.5 µA.

V. Summary and Conclusions

This paper has described the principle of operation of Programmable Metallization Cell memory and presented results from a variety of device structures. Ag-Ge-Se devices form 1 μm to 40 nm in diameter show highly promising characteristics, with both write and erase occurring at low voltage and current. On-state resistance is a function of write current and can be programmed from several hundred kΩ to close to 100 Ω, even in nanoscale devices. Such low resistance is of considerable use in non-memory applications, such as interconnection elements in programmable logic. A reduction in resistance of several orders of magnitude is attainable for a write power as low as 250 nW (I_{prog} = 1 μA), and 7.5 μW can create a highly persistent non-volatile state in which the extrapolated on-state resistance remains below 100 kΩ at 70°C for 10 years. The devices also show excellent endurance with no significant degradation to over 10^{10} cycles which implies stable operation well beyond this, possibly to over 10^{16} cycles. Although our test set up is non-ideal for high speed measurements, the results show that the devices switch within 35 nsec and a much higher intrinsic speed is presumed. Note that write times in the order of a few tens of nsec mean that the write energy is only 0.25 pJ even for a "hard" write at 30 μA and will of course be smaller for lower write current, which makes PMC one of the lowest energy memories. The sulfide-based devices have similar electrical characteristics to the selenide-based variants and appear to be tolerant to high processing temperatures which means that they may be more easily integrated into existing back end of line (BEOL) process schemes. Devices based on Ag- or Cu-doped WO_3 also show great promise as memory devices. The main advantage of this approach, particularly with Cu, is that materials that are already in use in advanced integrated circuits can be "converted" into embedded memory elements at very low cost.

The low resistivity of the electrodeposits means that even a nanoscale link of a few tens of nm in diameter, bridging an electrolyte a few tens of nm thick, will result in a resistance in the order of $10^4 - 10^5$ Ω. An electrodeposit this small means that the entire device can also be shrunk to nanoscale dimensions without compromising its operating characteristics. We have demostrated this by fabricating nanoscale devices and these behave much like their larger counterparts. This physical scalability, combined with low voltage and current operation, suggests that extremely high storage densities will be possible. The other benefit of forming a small volume electrodeposit is that it takes little charge to do so – as little as a few thousand deposited atoms will result in a stable low resistance link and this will require around 1 fC of charge. The charge required to switch a PMC element to a non-volatile low resistance state is therefore comparable to or lower than the charge required for *each* refresh cycle in a typical DRAM.

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